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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/917,290	07/27/2001	Faraydon O. Karim	00-LJ-217 (STMI01-00217)	8101

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EXAMINER	
O BRIEN, BARRY J	

ART UNIT	PAPER NUMBER
2183	5

DATE MAILED: 05/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

7

Office Action Summary	Application No.	Applicant(s)	
	09/917,290	KARIM ET AL.	
	Examiner	Art Unit	
	Barry J. O'Brien	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 7/27/01, 8/20/01, 10/15/01, 5/22/03.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-20 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 5.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed on record in the file: Preliminary Amendment as received on 8/20/01, Declaration and Fee as received on 10/15/01, and IDS as received on 5/22/03.

Specification

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

4. The applicant is requested to review the specification and update the status of all co-pending applications made mention of, replacing attorney docket numbers with current U.S. application or patent numbers when appropriate.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 5 and 12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. Claim 5, lines 3 and 4, recite the limitation "marks all fetched instruction". Please correct the claim language to read, "marks all fetched instructions" in order to be grammatically correct. See also a similar problem requiring correction in claim 12, lines 3 and 4.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Boufarah et al., U.S. Patent No. 5,127,091.

10. Regarding claims 1, 8 and 15, taking claim 8 as exemplary, Boufarah has taught a processor comprising:

a. At least one execution unit (20 of Fig.1),

b. A decode unit (20 of Fig.1, see Col.3 line 61 – Col.4 line 22),

c. A branch architecture for limiting branch penalty without branch prediction comprising:

I. A fetch-branch unit (14 of Fig.1) operating in parallel with the decode unit (see Fig.1) and controlling retrieval of instructions for the decode unit (see Col.3 lines 34-38), wherein the fetch-branch unit, upon detecting a branch instruction during one cycle,

i. Initiates retrieval of at least one sequential instruction from a location immediately following a location of a last retrieved instruction during one of a first cycle immediately following the one cycle and a second cycle immediately following the first cycle (see Col.7 lines 33-54, as well as Fig.2c, Fig.2d and Col.4 line 29 – Col.5 line 19),

ii. Initiates retrieval of at least one target instruction from a target location for the branch instruction during the other of the first cycle immediately following the one cycle and the second cycle immediately following the first cycle (see Col.7 lines 33-54, as well as Fig.2c, Fig.2d and Col.4 line 29 – Col.5 line 19).

11. Claims 1 and 15 are nearly identical to claim 8. Claim 1 differs in its lack of execution and decode units, but encompasses the same scope as claim 8. Claim 15 differs in it being comprised in a method, but encompasses the same scope as claim 8. Therefore, claims 1 and 15 are rejected for the same reasons as claim 8.

12. Regarding claims 2, 9 and 16, taking claim 9 as exemplary, Boufarah has taught the processor as set forth in claim 8, wherein the fetch-branch unit resolves the branch instruction and, upon resolving the branch instruction, drops either the at least one sequential instruction or the at least one target instruction (see Col.7 line 55 – Col.8 line 9).

13. Claims 2 and 16 are nearly identical to claim 9, differing only in their parent claims, but encompassing the same scope as claim 9. Therefore, claims 2 and 16 are rejected for the same reasons as claim 9.

14. Regarding claims 3, 10 and 17, taking claim 10 as exemplary, Boufarah has taught the processor as set forth in claim 9, wherein the fetch-branch unit, upon resolving the branch instruction, retrieves at least one instruction from a location immediately following a location of a last retrieved instruction within either the at least one sequential instruction or the at least one target instruction, depending upon whether a branch is taken (see Col.7 line 55 – Col.8 line 9).

15. Claims 3 and 17 are nearly identical to claim 10, differing only in their parent claims, but encompassing the same scope as claim 10. Therefore, claims 3 and 17 are rejected for the same reasons as claim 10.

16. Regarding claims 4, 11 and 18, taking claim 11 as exemplary, Boufarah has taught the processor as set forth in claim 9, wherein the fetch-branch unit, upon detecting a branch instruction during the one cycle, marks any fetched instruction preceding the branch instruction with a regular instruction type identifier (see "X1, X2" of Fig.2h), marks the branch instruction with a branch instruction type identifier (see "BRC" of Fig.2h), and marks any fetched instruction succeeding the branch instruction with a sequential instruction type identifier (see "S1, S2, S3" of Fig.2h). Here, while the processor of Boufarah has not explicitly taught "marking" the instructions with identifiers, Boufarah has taught the identification of fetched instructions as regular, branch, sequential, and target instructions, and thus inherently is "marking" the instructions so the processor can determine which instructions are which when it requires canceling of one of the fetch paths (see Col.5 line 61 – Col.6 line 39).

17. Claims 4 and 18 are nearly identical to claim 11, differing only in their parent claims, but encompassing the same scope as claim 11. Therefore, claims 4 and 17 are rejected for the same reasons as claim 11.

18. Regarding claims 5, 12 and 19, taking claim 12 as exemplary, Boufarah has taught the processor as set forth in claim 11, wherein the fetch-branch unit, upon not detecting a branch instruction during the one cycle, marks all fetched instruction with the regular instruction type identifier (see "X1, X2, X3" of Fig.2j). Here, while the processor of Boufarah has not explicitly taught "marking" the instructions with identifiers, Boufarah has taught the identification of fetched instructions as regular, branch, sequential, and target instructions, and thus inherently is "marking" the instructions so the processor can determine which instructions are which when it requires canceling of one of the fetch paths (see Col.6 line 40 – Col.7 line 13).

19. Claims 5 and 19 are nearly identical to claim 12, differing only in their parent claims, but encompassing the same scope as claim 12. Therefore, claims 5 and 19 are rejected for the same reasons as claim 12.

20. Regarding claims 6 and 13, taking claim 13 as exemplary, Boufarah has taught the processor as set forth in claim 8, wherein the fetch-branch unit marks the at least one sequential instruction with a sequential type identifier (see "S1, S2, S3" of Fig.2h). Here, while the processor of Boufarah has not explicitly taught "marking" the instructions with identifiers, Boufarah has taught the identification of fetched instructions as regular, branch, sequential, and target instructions, and thus inherently is "marking" the instructions so the processor can determine which instructions are which when it requires canceling of one of the fetch paths (see Col.5 line 61 – Col.6 line 39).

21. Claim 6 is nearly identical to claim 13, differing only in its parent claim, but encompassing the same scope as claim 13. Therefore, claim 6 is rejected for the same reasons as claim 13.

22. Regarding claims 7 and 14, taking claim 14 as exemplary, Boufarah has taught the processor as set forth in claim 8, wherein the fetch-branch unit marks the at least one target instruction with a target instruction type identifier (see "T1, T2, T3, T4" of Fig.2h). Here, while the processor of Boufarah has not explicitly taught "marking" the instructions with identifiers, Boufarah has taught the identification of fetched instructions as regular, branch, sequential, and target instructions, and thus inherently is "marking" the instructions so the processor can determine which instructions are which when it requires canceling of one of the fetch paths (see Col.5 line 61 – Col.6 line 39).

23. Claim 7 is nearly identical to claim 14, differing only in its parent claim, but encompassing the same scope as claim 14. Therefore, claim 7 is rejected for the same reasons as claim 14.

24. Regarding claim 20, Boufarah has taught the method as set forth in claim 15, further comprising:

a. Marking the at least one sequential instruction with a sequential instruction type identifier (see "S1, S2, S3" of Fig.2h),

b. Marking the at least one target instruction with a target instruction type identifier (see "T1, T2, T3, T4" of Fig.2h). Here, while the processor of Boufarah has not explicitly taught "marking" the instructions with identifiers, Boufarah has taught the identification of fetched instructions as regular, branch, sequential, and target instructions, and thus inherently is "marking" the instructions so the processor can determine which instructions are which when it requires canceling of one of the fetch paths (see Col.5 line 61 – Col.6 line 39).

Conclusion

25. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

26. Amerson et al., U.S. Patent No. 5,615,386, has taught a processor that fetches the cache lines containing both the sequential and target paths of a branch so that the correct path can be executed without using branch prediction.

27. Mowry et al., U.S. Patent No. 5,696,958, has taught a processor that initiates the fetching of both sequential and target paths of a branch instruction so that the correct stream can be executed without using branch prediction.

28. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Barry J. O'Brien whose telephone number is (703) 305-5864. The examiner can normally be reached on Mon.-Fri. 6:30am-4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

29. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Barry J. O'Brien
Examiner
Art Unit 2183

BJO
5/19/2004

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